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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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20457	7590	01/02/2004	EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/933,805	NINOMIYA ET AL.
	/Examiner Hetul Patel	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 November 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 21,23,24 and 26-42 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 21,23,24 and 26-42 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 08/814,625.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 a) The translation of the foreign language provisional application has been received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) Other: _____

Response to Amendment

1. This action is responsive to communication filed on November 26, 2003. This amendment has been entered and carefully considered. Claims 21, 23, 24 and 26 are again presented for examination. Claims 27-42 have been newly added for examination.
2. The objection to title is withdrawn due to the Amendment filed on November 26, 2003.
3. The objection to claim 23 is withdrawn due to the Amendment filed November 26, 2003.
4. The Double patenting rejection with respect to claims 21 and 24 is maintained and reiterated below.
5. Applicant's arguments filed on November 26, 2003 with respect to claims 21, 23, 24 and 26 have been fully considered but deemed to be moot in view of new ground rejection.

Claim Objections

6. Claim 34 is objected to because of the following informalities:
It should be stated as "... and adds a longitudinal redundancy check (LRC) code ..." instead of "... and adds an longitudinal redundancy check (LCD) code ..." as disclosed on page 7 of the communication filed on November 26, 2003.
Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 21 and 24 are rejected under the judicially created doctrine of double patenting over claims 1-2 of U. S. Patent No. 6,581,128 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

The applicant discloses a storage system comprising host adaptors, storage devices, disk adaptors, cache(s) and two buses having a transfer ability larger than one of said buses as described in the applicant's claims 21 and 24. It further includes a format converter as added in the amended claims. It also includes that the said memory can be referred to by an external processor as described in the applicant's claims 23 and 26.

The applicant claimed identical storage system in the claims 1 and 2 of the U. S. Patent No. 6,581,128, wherein each bus in said two buses is adapted to transfer different data. It is clearly obvious that the combined transfer ability of said two buses is larger than any one of said two buses as claimed in claims 21 and 24 of this application. It is also clearly obvious that a format converter must be added in between the host adaptors and storage devices because the host adaptors and storage devices accept data in different formats from each other.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application, which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 21, 23, 24, 26-33 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (USPN: 5,337,414), hereinafter Hashemi in view of Nakamura (USPN: 5,388,013).

As per claims 21, 24, 33 and 40, Hashemi teaches the invention as claimed, including a storage system comprising:

- a plurality of host adaptors coupled to at least one host device, which from interfaces for the host device (e.g. see figure 1, elements 4a-d and 8c1 and 8c2, column 3, lines 57-60 and 66-68; column 4, lines 1, 11-15 and column 9, lines 4-9);
- a plurality of storage devices for storing therein data received from the host device (e.g. see column 9, lines 30-34);
- a plurality of disk adaptors each coupled to one of said storage devices, which form interfaces for said storage devices (e.g. see figure 1, elements 8d1 and 8d2, column 4, lines 27-43; column 9, line 62 and column 10, lines 24-30);
- a cache (a plurality of caches) for temporarily storing therein data transferred between said plurality of host adaptors and said plurality of disk adaptors (e.g. see figure 1a, elements 24c1 or 24c2 or 24d1 or 24d2);
- two buses coupled to said plurality of host adaptors, said plurality of disk adaptors, and said cache, and which operate as a pair of buses for transferring data among said plurality of host adaptors, said plurality of disk adaptors, and said cache, wherein each bus in said two buses is adapted to transfer different data (e.g. see figure 1a, elements 6a-b), and a memory for storing a status of which of said two buses is available for use due to a failure in the other of said two buses (e.g. see column 9, lines 28-41).

Hashemi teaches the storage system as described above. However, Hashemi does not teach the further limitation of a format converter within said storage system. Nakamura, on the other hand, teaches the data storage format converter that is used

to convert a track of records of a variable length CKD format into records of a fixed length FBA format for storage (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to employ the format converter as taught by Nakamura in the storage system of Hashemi so the data stored in a first format (variable length record format adopted in a magnetic disc system of a general-purpose computer) sent from the host device can be converted into data of a second format (fixed length format which is adopted in a commercially available miniature type magnetic disc) suitable for the storage devices. By doing so, it would provide improved compatibility by allowing Hashemi's storage system (a) to serve broader range of applications, (b) to be compatible with wide variety of storage devices with different formats (e.g. Magnetic disks, optical disks, flash memory etc.)

As for claims 23 and 26, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches that said memory can be referred to by an external processor (e.g. see column 9, line 1 et seq.).

As per claims 27 and 37, Hashemi teaches the invention as claimed, including a storage system comprising:

- a plurality of first logical units coupled to at least one host device, which from interfaces for the host device (e.g. see figure 1, elements 4a-d and 8c1 and 8c2, column 3, lines 57-60 and 66-68; column 4, lines 1, 11-15 and column 9, lines 4-9);

- a plurality of storage devices for storing therein data transferred from the host device (e.g. see column 9, lines 30-34);
- a plurality of second logical units coupled to said storage devices (e.g. see figure 1, elements 8d1 and 8d2, column 4, lines 27-43; column 9, line 62 and column 10, lines 24-30);
- at least one cache memory unit (a plurality of caches) for temporarily storing therein data transferred between said plurality of first logical units and said plurality of second logical units (e.g. see figure 1a, elements 24c1 or 24c2 or 24d1 or 24d2); and
- at least one pass, coupled to said plurality of first logical units, said plurality of second logical units, and said at least one cache memory unit, which transfers data among said first logical units, said plurality of second logical units, and said at least one cache memory unit (e.g. see column 9, lines 28-41 and Fig. 1).

However, Hashemi does not teach the further limitation of a format converter and the cache memory unit that stores the data sent through said at least one pass. Nakamura, on the other hand, teaches the data storage format converter that is used to convert a track of records of a variable length CKD format into records of a fixed length FBA format for storage (e.g. see abstract). Nakamura also teaches the further limitation of having the cache memory unit that stores the data sent through said at least one pass (e.g. see Col. 10, line 40 to Col. 11, line 16). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to employ the format converter as taught by Nakamura in the storage system of Hashemi so the

data stored in a first format (variable length record format adopted in a magnetic disc system of a general-purpose computer) sent from the host device can be converted into data of a second format (fixed length format which is adopted in a commercially available miniature type magnetic disc) suitable for the storage devices. By doing so, it would provide improved compatibility by allowing Hashemi's storage system (a) to serve broader range of applications, (b) to be compatible with wide variety of storage devices with different formats (e.g. Magnetic disks, optical disks, flash memory etc.). By storing the data sent through said at least one pass into cache, it can increase the performance of the overall storage system since the cache is relatively faster than the storage devices. Therefore, the host devices can write the converted data into faster cache (use it as the intermediate buffer) and start processing the next data instead of waiting for the slower storage devices to copy the converted data into them.

As per claim 28, Hashemi discloses the claimed invention as described above. Hashemi does not teach that the format converter is provided in the plurality of first logical units. However, it would be further obvious to add a format converter in each of the first logical units so that the format conversion from the first format (CKD) to the second format (FBA) can be done in parallel fashion and therefore, while one of the plurality of the first logical units sends data to the format converter, the remaining of the plurality of the first logical units do not have to wait until the format converter finishes the first job. As a result, the performance of the overall storage system taught by the Hashemi can be increased.

As per claim 29, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system further comprising a shared memory unit (CIM/DIM in Figs. 1A and 1B) which stores therein control information for controlling the first logical units, the plurality of second logical units and said at least one cache memory unit. (e.g. see Col. 3, lines 24-33 and Figs. 1A and 1B).

As per claim 30, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system wherein said at least one cache memory unit (buffers 24c1-2 and 2d1-2 in Fig. 1A) has a plurality of cache memories arranged in a duplexed form, and the shared memory unit (CIM/DIM) has a plurality of shared memories arranged in a duplexed form (e.g. see Fig. 1A).

As per claims 31-32 and 38-39, Hashemi discloses the claimed invention as described above and furthermore, Hashemi teaches the storage system wherein said at least one pass (Futurebuses 6a and 6b in Fig. 1A) is a duplexed common bus, which includes:

- a control information bus coupled to the first logical units and the second logical units, which transfers control information, and
- a data transfer bus coupled to the first logical units, the second logical units and cache memory unit, which transfers data among the first logical units, the second logical units and cache memory unit (e.g. see Fig. 1A and Col. 3, lines 50-65).

9. Claims 34-35, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi in view Nakamura, further in view of Cheney et al. (USPN: 5,285,456), hereinafter, Cheney.

As per claims 34 and 41, the combination of Hashemi and Nakamura disclose the claimed invention as described above wherein the format converter converts data of CKD into data of FBA format. However, Hashemi and Nakamura fail to teach that the format converter adds a longitudinal redundancy check (LRC) code to the data of the FBA format. Cheney, on the other hand, teaches that by adding the LRC code to the data, integrity of the control information can be verified (e.g. see Col. 4, lines 9-14). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the storage system of Hashemi by adding the CRC code to the data as taught by Cheney. In doing so, it would allow the integrity of the information data and the control information to be verified when they are transferred within the system; therefore, enhancing the system's reliability.

As per claims 35 and 42, the combination of Hashemi and Nakamura disclose the claimed invention as described above. However, Hashemi and Nakamura fail to teach that the first logical units receive the physical address information in the CKD format with the cyclic redundancy check (CRC) code on a storage space of the storage device. Cheney, on the other hand, teaches that by adding the CRC code to the data, the errors generated during transmitting the data from the host devices to the storage devices can be detected (e.g. see Col. 2, lines 40-62). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to

modify the storage system of Hashemi by adding the CRC code to the data as taught by Cheney. In doing so, it would allow the integrity of the information data and the control information to be verified when they are transferred within the system; therefore, enhancing the system's reliability.

10. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi in view Nakamura, further in view of Dixon et al. (USPN: 4,637,024), hereinafter, Dixon.

As per claim 36, the combination of Hashemi and Nakamura disclose the claimed invention as described above. However, Hashemi and Nakamura, fail to teach that the format converter adds the ECC and CRC code to the data before writing it to the storage device. Dixon, on the other hand, teaches that by using the CRC code, the data can be checked/verified for any errors and if any error found in the data, using the ECC, that error can be fixed (e.g. see Col. 3, lines 24-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to employ the step of adding the ECC and CRC code to the data before storing it to the storage device as taught by Dixon in the system taught by Hashemi and Nakamura. In doing so, the data get checked and corrected before it get stored in the storage device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

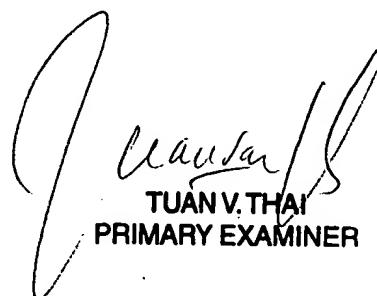
TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

HBP



TUAN V. THAI
PRIMARY EXAMINER